In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 1, lines 2 to 6 as follows:

--The present application is related to and claims priority from co-pending US provisional patent application entitled, "A Method for Easy FPGA Implementation of Designs with Complex Clockings", Filed: 4/25/03, Serial Number: 60/465,928, ~~Attorney Docket Number: TI-36308PS,~~ naming as inventors: NATARAJAN et al, and is incorporated in its entirety herewith into the present application.--

Rewrite paragraph [0024] as follows:

--[0024] Base sequential elements 110, 120, 150 and 160 implement a circuit logic when clocked according to the respective circuit clocks 111, 112, 115 and 116 respectively. Assuming that each base sequential element forms a D flip-flop, the data on paths 102, 103, 105, and 106 is provided on corresponding output paths 115, 125, 155 and 165 according to the corresponding circuit clock. It should be understood that the circuit clocks can be generated independently of or from a common system clock. --

Rewrite paragraph [0027] as follows:

--[0027] At time point ~~207[1] In~~ 220-1 in both this figure and Figure 5, it appears that 207 needs to be earlier than time point 210. In Figure 5 ~~you had proposed to change it~~ this is changed (possibly under the assumption that this time point is for the other input), the data on path 106 is changed from logic high to logic low (0). Before time point 210, data on paths 255 and 265 is shown at logic high (1). At time point 210, circuit clock 216 is shown going from 0 to 1, and circuit clock 215 is shown following to 1 at time point 220-1 with a skew of duration 250. Skew 250

between circuit clocks 116 and 115 is assumed to be caused by delay block 130. Ideally skew 250 should equal zero.--

Rewrite paragraph [0038] as follows:

--[0038] Edge detect block 410 generates an enable pulse (on path 413) for one clock cycle of global clock 350 on receiving a rising edge of circuit clock 115. The enable pulse is provided as select control signal 413 to multiplexor 430. The implementation of edge detect block 410 will be apparent to one skilled in the relevant arts by reading the disclosure provided herein. Base sequential element ~~150~~ 450 may operate similar to base sequential elements 110/120/150 and 160, and thus store a value received on path 405 at an (rising) edge of global clock 350.--

Rewrite paragraph [0040] as follows:

--[0040] As a result, the data available on path 105 is transferred only after the rising edge of circuit clock 105, but the time of transfer is controlled ~~bycloek~~ by clock 350. The description is continued with reference to a timing diagram illustrating the operation of the circuits of Figures 3 and 4 in further detail.--

Rewrite paragraph [0042] as follows:

--[0042] Figure 5 is a timing diagram illustrating the manner in which the problem(s) associated with Figures 1 and 2 may be addressed by the circuits of Figure 3 and 4. For conciseness, only the differences of Figure 5 as compared to Figure 2 are described for conciseness. In addition to the signals of Figure 2, the timing diagram of Figure 5 is shown depicting clock 550 (corresponding to global clock 350), select control signal 513 (path 413), ~~output565~~ output 565 (path 165 of Figure 4), and output 555 (path 155 of Figure 4). Each waveform is described in detail below.--